Degree competences to which the subject contributes

**Specific:**
1. Ability to design CMOS digital and analog integrated circuits of medium complexity.
2. Ability to apply low-power techniques to integrated circuits (ICs).
3. Ability to design for testability and test schemes for ICs.

**Transversal:**
4. EFFECTIVE USE OF INFORMATION RESOURCES: Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.
5. FOREIGN LANGUAGE: Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

**Teaching methodology**
- Lectures
- Laboratory classes
- Laboratory practical work
- Group work (distance)
- Oral presentations
- Short answer test (Control)
- Extended answer test (Final Exam)

**Learning objectives of the subject**

Learning objectives of the subject:

The aim of this course is to train students in methods of integrated circuit design. First, state-of-the-art and trends in VLSI and their design implications are introduced. Then, basic analog and digital circuits are presented. In a second phase, low-power techniques and design for testability are developed. Lab projects are proposed to introduce the practical aspects of VLSI design and the CAE tools.
Learning results of the subject:

- Ability to understand the evolution of integrated technologies.
- Ability to identify cases and applications suitable for an integrated solution.
- Ability to analyze the characteristics of a mixed-signal integrated circuit.
- Ability to design analog and digital medium-complexity CMOS integrated circuits.

Study load

<table>
<thead>
<tr>
<th>Total learning time: 125h</th>
<th>Hours large group: 26h</th>
<th>20.80%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hours medium group:</td>
<td>0h</td>
<td>0.00%</td>
</tr>
<tr>
<td>Hours small group:</td>
<td>13h</td>
<td>10.40%</td>
</tr>
<tr>
<td>Guided activities:</td>
<td>0h</td>
<td>0.00%</td>
</tr>
<tr>
<td>Self study:</td>
<td>86h</td>
<td>68.80%</td>
</tr>
</tbody>
</table>
# Content

## 1. Introduction

<table>
<thead>
<tr>
<th>Learning time: 8h</th>
</tr>
</thead>
<tbody>
<tr>
<td>Theory classes: 3h</td>
</tr>
<tr>
<td>Self study : 5h</td>
</tr>
</tbody>
</table>

**Description:**
- Structure of static gates.
- MOSFET models.
- State-of-the-art in VLSI. Full-custom and standard-cell design.

## 2. Basic digital blocks and their characterization

<table>
<thead>
<tr>
<th>Learning time: 20h</th>
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</thead>
<tbody>
<tr>
<td>Theory classes: 7h</td>
</tr>
<tr>
<td>Laboratory classes: 2h</td>
</tr>
<tr>
<td>Self study : 11h</td>
</tr>
</tbody>
</table>

**Description:**
- Parasitic elements. Delay definitions. Logical effort.
- Power dissipation.

## 3. Basic analog blocks and their characterization

<table>
<thead>
<tr>
<th>Learning time: 20h</th>
</tr>
</thead>
<tbody>
<tr>
<td>Theory classes: 7h</td>
</tr>
<tr>
<td>Laboratory classes: 2h</td>
</tr>
<tr>
<td>Self study : 11h</td>
</tr>
</tbody>
</table>

**Description:**
- Current sources and mirrors.
- Basic amplifier stages.
- Voltage and current references.
- Small-signal model. Parasitics and frequency response.
4. Practical aspects of VLSI design

<table>
<thead>
<tr>
<th>Learning time: 16h</th>
</tr>
</thead>
<tbody>
<tr>
<td>Theory classes: 5h</td>
</tr>
<tr>
<td>Laboratory classes: 2h</td>
</tr>
<tr>
<td>Self study: 9h</td>
</tr>
</tbody>
</table>

**Description:**
- Buffering.
- Power and clock distribution.
- Input/output pads. Packaging.
- Low-power circuit- and architecture-level techniques.

5. Basic concepts of testing

<table>
<thead>
<tr>
<th>Learning time: 12h</th>
</tr>
</thead>
<tbody>
<tr>
<td>Theory classes: 4h</td>
</tr>
<tr>
<td>Laboratory classes: 2h</td>
</tr>
<tr>
<td>Self study: 6h</td>
</tr>
</tbody>
</table>

**Description:**
- Design for testability. Test coverage. ATPG.
- Design for manufacturability.

6. Laboratory of VLSI design

<table>
<thead>
<tr>
<th>Learning time: 49h</th>
</tr>
</thead>
<tbody>
<tr>
<td>Laboratory classes: 5h</td>
</tr>
<tr>
<td>Self study: 44h</td>
</tr>
</tbody>
</table>

**Description:**
- Design of a transconductor.
- Design of a simple digital processor.
- Design project: digitally-assisted analog front-end.
Planning of activities

LABORATORY

Description:
- Introduction to CAE tools for VLSI. Design rules, layout, electric and logic simulation, synthesis, placement & routing, backannotation.
- Design of a transconductor.
- Design of a simple digital processor.
- Design project. Front-end and back-end.

ORAL PRESENTATION

Description:
Presentation of a work group.

SHORT ANSWER TEST (CONTROL)

Description:
Mid term control.

EXTENDED ANSWER TEST (FINAL EXAMINATION)

Description:
Final examination.

Qualification system

Final examination: 35%
Midterm examination: 35%
Laboratory assessments: 30%

Bibliography

Basic:

Complementary: