230646 - MND - Micro and Nano Electronic Design

Coordinating unit: 230 - ETSETB - Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering
Academic year: 2020
Degree: MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2013). (Teaching unit Compulsory)
MASTER'S DEGREE IN ADVANCED TELECOMMUNICATION TECHNOLOGIES (Syllabus 2019). (Teaching unit Optional)
MASTER'S DEGREE IN TELECOMMUNICATIONS ENGINEERING (Syllabus 2013). (Teaching unit Optional)
ECTS credits: 5
Teaching languages: English

Teaching staff

Coordinator: JORDI MADRENAS BOADAS
Others: FRANCESC MOLL ECHETO, JORDI COSP VILELLA
Madrenas Boadas, Jordi

Degree competences to which the subject contributes

Specific:
1. Ability to design CMOS digital and analog integrated circuits of medium complexity.
2. Ability to apply low-power techniques to integrated circuits (ICs).
3. Ability to design for testability and test schemes for ICs.

Transversal:
4. EFFECTIVE USE OF INFORMATION RESOURCES: Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.
5. FOREIGN LANGUAGE: Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

Teaching methodology

- Lectures
- Laboratory classes
- Laboratory practical work
- Group work (distance)
- Oral presentations
- Short answer test (Control)
- Extended answer test (Final Exam)

Learning objectives of the subject

Learning objectives of the subject:

The aim of this course is to train students in methods of integrated circuit design. First, state-of-the-art and trends in VLSI and their design implications are introduced. Then, basic analog and digital circuits are presented. In a second phase, low-power techniques and design for testability are developed. Lab projects are proposed to introduce the practical aspects of VLSI design and the CAE tools.
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Learning results of the subject:

- Ability to understand the evolution of integrated technologies.
- Ability to identify cases and applications suitable for an integrated solution.
- Ability to analyze the characteristics of a mixed-signal integrated circuit.
- Ability to design analog and digital medium-complexity CMOS integrated circuits.

<table>
<thead>
<tr>
<th>Study load</th>
<th>Hours large group:</th>
<th>26h</th>
<th>20.80%</th>
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<tbody>
<tr>
<td></td>
<td>Hours medium group:</td>
<td>0h</td>
<td>0.00%</td>
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<tr>
<td></td>
<td>Hours small group:</td>
<td>13h</td>
<td>10.40%</td>
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<td></td>
<td>Guided activities:</td>
<td>0h</td>
<td>0.00%</td>
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<tr>
<td></td>
<td>Self study:</td>
<td>86h</td>
<td>68.80%</td>
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</table>
# Content

<table>
<thead>
<tr>
<th>1. Introduction</th>
<th><strong>Learning time:</strong> 8h</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Description:</strong></td>
<td></td>
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<tr>
<td>- Structure of static gates.</td>
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<tr>
<td>- MOSFET models.</td>
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<tr>
<td>- State-of-the-art in VLSI. Full-custom and standard-cell design.</td>
<td>Theory classes: 3h</td>
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<td>Self study: 5h</td>
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<table>
<thead>
<tr>
<th>2. Basic digital blocks and their characterization</th>
<th><strong>Learning time:</strong> 20h</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Description:</strong></td>
<td></td>
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<tr>
<td>- The CMOS inverter. The NAND and NOR gates. Pass transistors. Tri-state.</td>
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<tr>
<td>- Parasitic elements. Delay definitions. Logical effort.</td>
<td></td>
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<tr>
<td>- Power dissipation.</td>
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<tr>
<th>3. Basic analog blocks and their characterization</th>
<th><strong>Learning time:</strong> 20h</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Description:</strong></td>
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<tr>
<td>- Current sources and mirrors.</td>
<td></td>
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<td>- Basic amplifier stages.</td>
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<tr>
<td>- Voltage and current references.</td>
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<td>- Small-signal model. Parasitics and frequency response.</td>
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</tbody>
</table>
### 4. Practical aspects of VLSI design

**Description:**
- Buffering.
- Power and clock distribution.
- Input/output pads. Packaging.
- Low-power circuit- and architecture-level techniques.

**Learning time:** 16h  
- Theory classes: 5h  
- Laboratory classes: 2h  
- Self study: 9h

### 5. Basic concepts of testing

**Description:**
- Design for testability. Test coverage. ATPG.
- Design for manufacturability.

**Learning time:** 12h  
- Theory classes: 4h  
- Laboratory classes: 2h  
- Self study: 6h

### 6. Laboratory of VLSI design

**Description:**
- Design of a transconductor.
- Design of a simple digital processor.
- Design project: digitally-assisted analog front-end.

**Learning time:** 49h  
- Laboratory classes: 5h  
- Self study: 44h
# Planning of activities

## LABORATORY

**Description:**
- Introduction to CAE tools for VLSI. Design rules, layout, electric and logic simulation, synthesis, placement & routing, backannotation.
- Design of a transconductor.
- Design of a simple digital processor.
- Design project. Front-end and back-end.

## ORAL PRESENTATION

**Description:**
Presentation of a work group.

## SHORT ANSWER TEST (CONTROL)

**Description:**
Mid term control.

## EXTENDED ANSWER TEST (FINAL EXAMINATION)

**Description:**
Final examination.

## Qualification system

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>Final examination</td>
<td>35%</td>
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<tr>
<td>Midterm examination</td>
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<tr>
<td>Laboratory assessments</td>
<td>30%</td>
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## Bibliography

**Basic:**


**Complementary:**
