Degree competences to which the subject contributes

Specific:
1. Ability to design CMOS digital and analog integrated circuits of medium complexity.
2. Ability to apply low-power techniques to integrated circuits (ICs).
3. Ability to design for testability and test schemes for ICs.

Transversal:
4. EFFECTIVE USE OF INFORMATION RESOURCES: Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.
5. FOREIGN LANGUAGE: Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

Teaching methodology

- Lectures
- Laboratory classes
- Laboratory practical work
- Group work (distance)
- Oral presentations
- Short answer test (Control)
- Extended answer test (Final Exam)

Learning objectives of the subject

The aim of this course is to train students in methods of integrated circuit design. First, state-of-the-art and trends in VLSI and their design implications are introduced. Then, basic analog and digital circuits are presented. In a second phase, low-power techniques and design for testability are developed. Lab projects are proposed to introduce the practical aspects of VLSI design and the CAE tools.
Learning results of the subject:

- Ability to understand the evolution of integrated technologies.
- Ability to identify cases and applications suitable for an integrated solution.
- Ability to analyze the characteristics of a mixed-signal integrated circuit.
- Ability to design analog and digital medium-complexity CMOS integrated circuits.

**Study load**

<table>
<thead>
<tr>
<th>Total learning time: 125h</th>
<th>Hours large group: 26h</th>
<th>20.80%</th>
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<tbody>
<tr>
<td></td>
<td>Hours medium group: 0h</td>
<td>0.00%</td>
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<tr>
<td></td>
<td>Hours small group: 13h</td>
<td>10.40%</td>
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<td></td>
<td>Guided activities: 0h</td>
<td>0.00%</td>
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<tr>
<td></td>
<td>Self study: 86h</td>
<td>68.80%</td>
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</table>
## Content

<table>
<thead>
<tr>
<th>Section</th>
<th>Description</th>
<th>Learning time:</th>
<th>Theory classes:</th>
<th>Laboratory classes:</th>
<th>Self study:</th>
</tr>
</thead>
</table>
| **1. Introduction** | - Structure of static gates.  
- MOSFET models.  
- State-of-the-art in VLSI. Full-custom and standard-cell design. | 8h | 3h | | 5h |

### Description:
- Structure of static gates.  
- MOSFET models.  
- State-of-the-art in VLSI. Full-custom and standard-cell design.

| **2. Basic digital blocks and their characterization** | Description:  
- Parasitic elements. Delay definitions. Logical effort.  
- Power dissipation. | 20h | 7h | 2h | 11h |

### Description:
- Parasitic elements. Delay definitions. Logical effort.  
- Power dissipation.

| **3. Basic analog blocks and their characterization** | Description:  
- Current sources and mirrors.  
- Basic amplifier stages.  
- Voltage and current references.  
- Small-signal model. Parasitics and frequency response. | 20h | 7h | 2h | 11h |

### Description:
- Current sources and mirrors.  
- Basic amplifier stages.  
- Voltage and current references.  
- Small-signal model. Parasitics and frequency response.
| **4. Practical aspects of VLSI design** | **Learning time:** 16h  
Theory classes: 5h  
Laboratory classes: 2h  
Self study: 9h |
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<tbody>
<tr>
<td><strong>Description:</strong></td>
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<tr>
<td>- Buffering.</td>
<td></td>
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<tr>
<td>- Power and clock distribution.</td>
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<tr>
<td>- Input/output pads. Packaging.</td>
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<tr>
<td>- Low-power circuit- and architecture-level techniques.</td>
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</tbody>
</table>

| **5. Basic concepts of testing** | **Learning time:** 12h  
Theory classes: 4h  
Laboratory classes: 2h  
Self study: 6h |
<table>
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<tbody>
<tr>
<td><strong>Description:</strong></td>
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</tbody>
</table>
| - Definitions.  
Manufacturing test.  
Defects and faults. |                                               |
| - Design for testability.  
Test coverage.  
ATPG. |                                               |
| - Self-test.  
Fault tolerance.  
System-level test. |                                               |
| - Design for manufacturability.   |                                               |

| **6. Laboratory of VLSI design** | **Learning time:** 49h  
Laboratory classes: 5h  
Self study: 44h |
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<tr>
<td><strong>Description:</strong></td>
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</table>
| - Introduction to CAE tools for VLSI.  
Layout editor.  
Electric and logic simulation.  
Synthesis.  
Placement & routing.  
Post-layout simulation. |                                               |
| - Design of a transconductor.     |                                               |
| - Design of a simple digital processor. |                                               |
| - Design project: digitally-assisted analog front-end. | |

---
# Planning of activities

## LABORATORY

**Description:**
- Introduction to CAE tools for VLSI. Design rules, layout, electric and logic simulation, synthesis, placement & routing, backannotation.
- Design of a transconductor.
- Design of a simple digital processor.
- Design project. Front-end and back-end.

## ORAL PRESENTATION

**Description:**
Presentation of a work group.

## SHORT ANSWER TEST (CONTROL)

**Description:**
Mid term control.

## EXTENDED ANSWER TEST (FINAL EXAMINATION)

**Description:**
Final examination.

## Qualification system

- Final examination: 35%
- Midterm examination: 35%
- Laboratory assessments: 30%

## Bibliography

**Basic:**


**Complementary:**
