## 230652 - ESDC - Electronic System Design for Communications

<table>
<thead>
<tr>
<th>Coordinating unit:</th>
<th>230 - ETSETB - Barcelona School of Telecommunications Engineering</th>
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</thead>
<tbody>
<tr>
<td>Teaching unit:</td>
<td>710 - EEL - Department of Electronic Engineering</td>
</tr>
<tr>
<td>Academic year:</td>
<td>2017</td>
</tr>
<tr>
<td>Degree:</td>
<td>MASTER'S DEGREE IN TELECOMMUNICATIONS ENGINEERING (Syllabus 2013). (Teaching unit Compulsory)</td>
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<tr>
<td>ECTS credits:</td>
<td>5</td>
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<tr>
<td>Teaching languages:</td>
<td>English</td>
</tr>
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### Teaching staff

<table>
<thead>
<tr>
<th>Coordinator:</th>
<th>Rubio Sola, Jose Antonio</th>
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<tbody>
<tr>
<td></td>
<td>Moll Echeto, Francesc De Borja</td>
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<tr>
<th>Others:</th>
<th>Rubio Sola, Jose Antonio</th>
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<tr>
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<td>Moll Echeto, Francesc De Borja</td>
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### Opening hours

| Timetable: | see consultation schedule for each professor in the web of the faculty |


Prior skills

Previous knowledge needed to follow all the explanations:

**CONCEPTS OF PHYSICS:**
- Plate parallel capacitance. Voltage-Charge relation. Dielectrics.
- PN Junctions: forward and reverse biasing.

**BASIC CIRCUIT ANALYSIS:**
- Concept of resonance frequency in RLC circuits.

**MOS TRANSISTOR**
- Identification of terminals, sign of currents and voltages in NMOS and PMOS devices.
- Large Signal (DC), long channel equations (ID vs VGS, VDS) curves and regions. Transconductance and gate dimensions. Channel-Length modulation.

**Overdrive voltage**
- Unified model for PMOS and NMOS.
- Threshold voltage effects: Body Effect. Threshold voltage as a function of bulksource voltage: linear simplification equation. Drain induced barrier lowering.
- Short channel equations: Mobility degradation and Velocity saturation.
- Parasitic capacitances: Gate capacitance and Diffusion Capacitance.

**DIGITAL CIRCUITS**
- CMOS Logic gates. Extraction of the truth table and logic expression form a gate transistor schematic.
- Pass Transistor DC characteristics. N, P and CMOS transmission gates.
- Inverter: Static transfer function. Noise Margin definition.

**DIGITAL DESIGN**
- State Machines: state diagram. Canonical structure of sequential systems.
- Digital waveform as a function of time interpretation.
- VHDL Hardware Description Language.
- Basic understanding of C programming
- Basic microprocessor experience

**DATA COMMUNICATIONS BASICS (*)&
- Basics of data flow and digital communication channels
- Network types (LAN, WLAN)
- Switched WAN
- Packet switching Networks
- Internet basics
- Communication protocols
- Protocols layering
- TCP/IP protocol
- Layers communication in networks with switching and routers
- Message encapsulation and decapsulation
- Addressing in TCP/IP protocol suite
Degree competences to which the subject contributes

Specific:
1. Ability to design and manufacture integrated circuits

2. Knowledge of hardware description languages for high-complex circuits.

3. Ability to use programmable logical devices, as well as to design analog and digital advanced electronics systems. Ability to design communication devices, such as routers, switches, hubs, transmitters and receivers in different bands.

Transversal:
4. EFFECTIVE USE OF INFORMATION RESOURCES: Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.
5. FOREIGN LANGUAGE: Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

Teaching methodology

- Lectures
- Application classes
- Laboratory activities
- Individual work
- Exercises
- Extended answer test (Final Exam)

Learning objectives of the subject

Learning objectives of the subject:

To understand the general principles and design methods of integrated electronic computing and communication systems.

Learning results of the subject:

- Ability to understand the design process of an integrated circuit.
- Ability to assess the possibilities and limitations of CMOS technology.
- Ability to design at circuit level the main subsystems of a digital electronic circuit based on given specifications, including communications applications.
- To acquire knowledge on signal integrity, power consumption and test of an electronic system.
## Study load

<table>
<thead>
<tr>
<th></th>
<th>Hours large group</th>
<th>Hours medium group</th>
<th>Hours small group</th>
<th>Guided activities</th>
<th>Self study</th>
<th>Percentage</th>
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<tbody>
<tr>
<td><strong>Total learning time</strong></td>
<td>125h</td>
<td>26h</td>
<td>0h</td>
<td>0h</td>
<td>86h</td>
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<td>13h</td>
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<td>68.80%</td>
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# Content

<table>
<thead>
<tr>
<th>Section</th>
<th>Learning time:</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>II. Delay in Digital Circuits</td>
<td>6h</td>
<td>Delay estimation in Digital Circuits. Maximum working frequency. Data Throughput. Design strategies to increase circuit performances.</td>
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<tr>
<td><strong>V: New technology challenges.</strong></td>
<td><strong>Learning time:</strong> 4h</td>
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<tr>
<td><strong>Description:</strong> Test of digital circuits. New technologies and technology challenges. More than Moore.</td>
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<tr>
<td>Theory classes: 2h</td>
<td>Self study: 2h</td>
<td></td>
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<thead>
<tr>
<th><strong>VI: Electronic technology evolution and progress in integrated circuits for data communication.</strong></th>
<th><strong>Learning time:</strong> 2h</th>
</tr>
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<tbody>
<tr>
<td><strong>Description:</strong> Electronic technology evolution and progress in integrated circuits for data communication. Recall of TCP/IP protocol and layers as well as the required main electronic functions at data and network levels: switchers and routers.</td>
<td></td>
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<tr>
<td>Theory classes: 2h</td>
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<tr>
<th><strong>VI: INTRODUCTION TO ELECTRONICS FOR COMMUNICATIONS</strong></th>
<th><strong>Learning time:</strong> 4h</th>
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<tr>
<td><strong>Description:</strong> Electronic technology evolution and progress in integrated circuits for data communication. Recall of TCP/IP protocol and layers as well as the required main electronic functions at data and network levels: switchers and routers.</td>
<td></td>
</tr>
<tr>
<td>Theory classes: 2h</td>
<td>Self study: 2h</td>
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<tr>
<th><strong>VII: SEMICONDUCTOR MEMORIES</strong></th>
<th><strong>Learning time:</strong> 4h</th>
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<tr>
<td><strong>Description:</strong> Semiconductor memories, advanced FIFO design (queues), queue modeling, system dimensioning. Focus on SRAM 6T cell memories, design, layout, circuits, system.</td>
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<tr>
<td>Theory classes: 2h</td>
<td>Self study: 2h</td>
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### VIII: SWITCHERS AND ROUTERS

**Learning time:** 4h  
Theory classes: 2h  
Self study: 2h  

**Description:**  
Packet switching. Switch fabric, transmission gate devices. Switch types and design, regular, multi-stage, Clos condition to avoid blocking. Other advanced switcher architectures: with time-slot interchange (TSI), time-space-time (TST), banyan-type, based on direct memory access (DMA).

### IX: DATA COMMUNICATION PERIPHERALS AND ARCHITECTURES

**Learning time:** 4h  
Theory classes: 2h  
Self study: 2h  

**Description:**  
CRC-circuit implementation. Data communication architectures and protocols: organization into data and control planes. Finite state machines design.

### Chapter X: ADVANCED NETWORK PROCESSORS

**Learning time:** 4h  
Theory classes: 2h  
Self study: 2h  

**Description:**  
Network processors (NP): motivation, state of the art (Intel, Broadcom, Cisco, Agere, IBM, Motorola, Clearwater, EZchip. Organization, performances.
### Planning of activities

#### EXERCISES

**Description:**
Exercises to strengthen the theoretical knowledge.

#### EXTENDED ANSWER TEST (FINAL EXAMINATION):

**Description:**
Final examination.

#### LABORATORY

**Hours:** 24h
- Self study: 12h
- Laboratory classes: 12h

**Description:**
The laboratory part is based on the Xilinx Zynq device: an FPGA with embedded processor. You will use a commercial development board called Zedboard.
The course consists in 4 Labs, the first three are guided and the last one consists on a design proposed by the professor.

**Descriptions of the assignments due and their relation to the assessment:**
- **Lab 1:** Simple embedded design.
  Introduction to the design with the Zedboard. Device configuration and simple application program. (2 weeks).

- **Lab 2:** Custom IP design.
  You will design a simple IP in the FPGA of the device to be used together with the embedded processor. (2 weeks).

- **Lab 3:** Ethernet configuration.
  You will learn how to configure and use the ethernet interface of the device, communicating with the PC. (2 weeks).

- **Lab 4:** Small design.
  Proposed by the professor, it usually involves the use of the communications interface available in the Zedboard. Collaboration between teams may be required. (6 weeks).

### Qualification system

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>Final examination</td>
<td>33%</td>
</tr>
<tr>
<td>Partial exams</td>
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<tr>
<td>Individual assessments</td>
<td>20%</td>
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<tr>
<td>Laboratory</td>
<td>33%</td>
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Bibliography

Basic:


Complementary: