230652 - ESDC - Electronic System Design for Communications

Coordinating unit: 230 - ETSETB - Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering
Academic year: 2020
Degree: MASTER'S DEGREE IN TELECOMMUNICATIONS ENGINEERING (Syllabus 2013). (Teaching unit Compulsory)
MASTER'S DEGREE IN ADVANCED TELECOMMUNICATION TECHNOLOGIES (Syllabus 2019). (Teaching unit Optional)
ECTS credits: 5
Teaching languages: English

Teaching staff
Coordinator: Rubio Sola, Jose Antonio
Moll Echeto, Francesc De Borja
Altet Sanahujes, Josep
Others: Rubio Sola, Jose Antonio
Moll Echeto, Francesc De Borja
Altet Sanahujes, Josep

Opening hours
Timetable: see consultation schedule for each professor
Prior skills

Previous knowledge needed to follow all the explanations:

CONCEPTS OF PHYSICS:
- Plate parallel capacitance. Voltage-Charge relation. Dielectrics.
- PN junctions: forward and reverse biasing.

BASIC CIRCUIT ANALYSIS:
- Concept of resonance frequency in RLC circuits.

MOS TRANSISTOR
- Identification of terminals, sign of currents and voltages in NMOS and PMOS devices.
- Large Signal (DC), long channel equations (ID vs VGS, VDS) curves and regions. Transconductance and gate dimensions. Channel-Length modulation.
- Overdrive voltage:
  - Unified model for PMOS and NMOS.
  - Threshold voltage effects: Body Effect. Threshold voltage as a function of bulk/source voltage: linear simplification equation. Drain induced barrier lowering.
  - Short channel equations: Mobility degradation and Velocity saturation.
  - Parasitic capacitances: Gate capacitance and Diffusion Capacitance

DIGITAL CIRCUITS
- CMOS Logic gates. Extraction of the truth table and logic expression form a gate transistor schematic.
- Pass Transistor DC characteristics. N, P and CMOS transmission gates.
- Inverter: Static transfer function. Noise Margin definition.

DIGITAL DESIGN
- State Machines: state diagram. Canonical structure of sequential systems.
- Basic combinational and sequential blocks. Truth table. Logic level schematic.
- Symbol. (basic logic gates, multiplexer, decoder, half adder, full adder, flip-flop, latch, register, counter).
- Digital waveform as a function of time interpretation.
- VHDL Hardware Description Language.
- Basic understanding of C programming
- Basic microprocessor experience

DATA COMMUNICATIONS BASICS (*):
- Basics of data flow and digital communication channels
- Types of network connections
- Network topologies
- Network types (LAN, WLAN)
- Switched WAN
- Packet switching Networks
- Internet basics
- Communication protocols
- Protocols layering
- TCP/IP protocol
- Layers communication in networks with switching and routers
- Message encapsulation and decapsulation
- Addressing in TCP/IP protocol suite
Degree competences to which the subject contributes

Specific:
1. Ability to design and manufacture integrated circuits
2. Knowledge of hardware description languages for high-complex circuits.
3. Ability to use programmable logical devices, as well as to design analog and digital advanced electronics systems. Ability to design communication devices, such as routers, switches, hubs, transmitters and receivers in different bands.

Transversal:
4. EFFECTIVE USE OF INFORMATION RESOURCES: Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.
5. FOREIGN LANGUAGE: Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

Teaching methodology
- Lectures
- Application classes
- Laboratory activities
- Individual work
- Exercises
- Extended answer test (Final Exam)

Learning objectives of the subject
Learning objectives of the subject:
To understand the general principles and design methods of integrated electronic computing and communication systems.

Learning results of the subject:
- Ability to understand the design process of an integrated circuit.
- Ability to assess the possibilities and limitations of CMOS technology.
- Ability to design at circuit level the main subsystems of a digital electronic circuit based on given specifications, including communications applications.
- To acquire knowledge on signal integrity, power consumption and test of an electronic system.
# Study load

<table>
<thead>
<tr>
<th>Total learning time: 125h</th>
<th>Hours large group: 26h 20.80%</th>
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<tbody>
<tr>
<td></td>
<td>Hours medium group: 0h 0.00%</td>
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<tr>
<td></td>
<td>Hours small group: 13h 10.40%</td>
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<td></td>
<td>Guided activities: 0h 0.00%</td>
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<tr>
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<td>Self study: 86h 68.80%</td>
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## Content

### Design Methodology

**Description:**
- Embedded system design
- Introduction: Objectives Part 1
- Digital blocks Review

**DESIGN METHODOLOGY**
- Design Structure
  - From specs to hardware description
  - VHDL implementation
- Concurrent vs. blocking operation
- Software design
- Concurrent Software State Machines
- New hardware design
- Design Lab3: Serial Communications

**Learning time:** 16h
- Theory classes: 8h
- Self study: 8h

### Specific communication electronic components and architectures

**Description:**
- Motivation, Basics of Digital Communications, Switch
- Queues and CRC Checkers/Generators
- Design of basic communication systems
- State of the art in R&D on Electronics for Communication

**Learning time:** 16h
- Theory classes: 8h
- Self study: 8h

### Integrated Circuit Design Concepts

**Description:**
- Delay in digital circuits. Timing analysis.
- Power and energy in integrated circuits.
- Low power design techniques.

**Learning time:** 16h
- Theory classes: 8h
- Self study: 8h
### Planning of activities

<table>
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<tr>
<th>EXERCISES</th>
<th>Description: Exercises to strengthen the theoretical knowledge.</th>
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<tbody>
<tr>
<td>LABORATORY</td>
<td>Description: The laboratory part is based on the Xilinx Zynq device: an FPGA with embedded processor. You will use a commercial development board. The course consists in 4 Labs, the first three are guided with a last section consisting on an independent design. Lab 4 consists on a design proposed by the professor.</td>
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</tbody>
</table>
| **Hours**: 74h    | Laboratory classes: 12h  
|                  | Self study: 62h  |
| **Exercises**    | **Self study**     |
| **Lab 1**: Simple embedded design.  
| Introduction to the design with Vivado. Device configuration and simple application program. (2 weeks). |
| **Lab 2**: Designing concurrent functions in software  
| You will design in an embedded system as the Zynq a programming strategy for concurrent functions. (2 weeks). |
| **Lab 3**: Full hardware design and serial communications  
| You will learn how to use a serial communications IP to communicate between two boards (2 weeks). |
| **Lab 4**: Small design.  
| Proposed by the professor, it usually involves the use of the communications interface. Collaboration between teams may be required. (6 weeks). |

### Qualification system

- **Final examination**: 47%
- **Partial exams**: 20%
- **Laboratory**: 33%
Bibliography

Basic:


Complementary: